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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	3
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Complete If Known

Application Number	10/708,056
Filing Date	February 5, 2004
First Named Inventor	Edmund M. Clarke
Art Unit	2825
Examiner Name	Siek V.
Attorney Docket Number	361007-000031

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

Examiner Initials ¹	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	To
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

**Examiner
Signature**

VUTHE SIEK

Date _____

Considered

6/27/06

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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete If Known			
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		Filing Date	February 5, 2004		
		First Named Inventor	Edmund M. Clarke		
		Art Unit	2825		
		Examiner Name			
Sheet	2	of	3	Attorney Docket Number	361007-000031

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
VS	B	Carl Pixley, Guest Editor's Introduction: Formal Verification of Commercial Integrated Circuits. IEEE Design & Test of Computers, 18(4):4-5, 2001.	
VS	C	Armin Biere, Alessandro Cimatti, Edmund M. Clarke, and Yunshan Yhu. Symbolic model checking without BDDs. In Tools and Algorithms for Construction and Analysis of Systems, pages 193-207, 1999.	
VS	D	A. Biere, E. Clarke, R. Raimi, and Y. Zhu. Verifying safety properties of a Power PC TM microprocessor using symbolic model checking without BDDs. In N. Halbwachs and D. Peled, editors, Proceedings of the 11 th International Conference on Computer Aided Verification (CAB 99), Lecture Notes in Computer Science. Springer Verlag, 1999.	
VS	E	A. Biere, A. Cimatti, E.M. Clarke, M. Fujita, and Y. Zhu. Symbolic model checking using SAT procedures instead of BDDs. In Design Automation Conference (DAC '99), 1999.	
VS	F	Joao P. Marques-Silva and Karem A. Sakallah. GRASP - A New Search Algorithm for Satisfiability. In Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pages 220-227, November 1996.	
	G	Matthew W. Moskwicz, Conor F. Madigan, Ying Zhao, Lintao Zhang, and Sharad Malik. Chaff: Engineering an efficient SAT solver. In Proceedings of the 38 th Design Automation Conference (DAC '01), June 2001.	
VS	H	D. Kroening and O. Strichman. Efficient computation of recurrence diameters. In Proceedings of the Fourth International Conference on Verification, Model Checking and Abstract Interpretation. Springer, 2003. To appear.	
VS	I	O. Strichman. Tuning SAT checkers for bounded model checking. In E.A. Emerson and A.P. Sistla, editors, Proceedings of the 12 th International Conference on Computer Aided Verification (CAV 2000), Lecture Notes in Computer Science. Springer Verlag, 2000.	
VS	J	Fady Cooty, Limor Fix, Ranan Fraer, Enrico Giunchiglia, Gila Kamhi, Armando Tacchella, and Moshe Y. Vardi. Benefits of bounded model checking at an industrial setting. In Gerard Berry, Hubert Comon, and Alain Finkel, editors, Proceedings of the 13 th International Conference on Computer Aided Verification (CAV 2001), number 2102 in Lecture Notes in Computer Science, pages 436-453. Springer Verlag, 2001.	
K	K	Per Bjesse, Tim Leonard, and Abdel Mokkedem. Finding bugs in an Alpha microprocessor using satisfiability solvers. In Gerard Berry, Hubert Comon, and Alain Finkel, editors, Proceedings of the 13 th International Conference on Computer Aided Verification (CAV 2001), number 2102 in Lecture Notes in Computer Science, pages 454-464. Springer Verlag, 2001.	

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				Attorney Docket Number	361007-000031

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✓	L	Luc Semeria, Andrew Seawright, Renu Mehra, Daniel Ng, Arjuna Ekanayake, and Barry Pangre. RTL C-based methodology for designing and verifying a multi-threaded processor. In Proc. Of the 39 th Design-Automation Conference ACM Press, 2002.	
VS	M	I. Page. Constructing Hardware-Software Systems from a Single Description. Journal of VLSI Signal Processing, 129(1):87-107, 1996.	
VS	N	A. Pnueli, M. Siegel, and O. Shtrichman. The code validation tool (CVT) – automatic verification of a compilation process. Int. Journal of Software Tools for Technology Transfer (STTT), 2(2):192-201, 1998.	
VS	O	R. Cytron, J. Ferrante, B.K. Rosen, M.N. Wegman, and F.K. Zadeck. An efficient method of computing static single assignment form. In Proceedings of the 16 th ACM SIGPLAN-SIGACT symposium on Principles of programming languages, pages 25-35. ACM Press, 1989.	
VS	P	David W. Currie, Alan J. Hu, and Sreeranga Rajan. Automatic formal verification of dsp software. In Proceedings of the 37 th Design Automation Conference (DAC 2000), pages 130-135. ACM Press, 2000.	
VS	Q	Kiyoharu Hamaguchi. Symbolic simulation heuristics for high-level design descriptions with uninterpreted functions. In International Workshop on High-Level Design, Validation, and Test, pages 25-30. IEEE, 2001.	
VS	R	C. Blank, H. Eveking, J. Levihn, and G. Ritter. Symbolic simulation techniques – state of the art and applications. In International Workshop on High-Level Design, Validation, and Test, pages 45-50. IEEE, 2001.	
	S	Apt. Krzysztof R. Logic and Models of Concurrent Systems, NATO ASI Series, Series F: Computer and System Sciences, Vol. 13. (No document)	

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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First Named Inventor	Edmund M. Clarke
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Examiner Name	Not Assigned
Attorney Docket Number	361007-000031

Sheet	1	of	2
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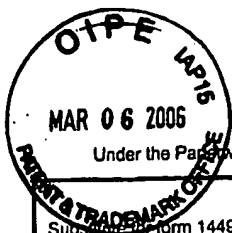
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VS	A	CLARKE, Edmund M. Jr., et al., Model Checking, (1999) United States, 33 pages.	

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